IN THE SPECIFICATION:

Please amend the specification as follows:

Please replace the paragraph beginning on page 5, line 8, with the following paragraph:

From another aspect of this invention, there is provided a process for producing a semiconductor apparatus, comprising the steps of (a) forming through holes at a first pitch in a support substrate, (b)forming an insulation layer on side walls of said through holes, (c) filling through holes filled with conductor in the through holes provided with said insulation film, (d) forming capacitors connected with at least some of said through holes filled with conductor, and wires connected with said through holes filled with conductor or said capacitors and having a second pitch, on said support substrate, and (e) connecting plural semiconductor elements having terminals in conformity with said second pitch, with said wires.

Please replace the paragraph beginning on page 8, line 23, with the following paragraph.

In the case where the via holes are small in diameter, the through holes filled with conductor can also be formed by CVD instead of plating. In this case, the seed layer is not especially necessary, and for example, CVD can be carried out in the state of Figs. 1B or 1C.

Please replace the paragraph beginning on page 9, line 1, with the following paragraph.

As shown in Fig. 1F, the upper surface of the Si substrate is flattened or planarized by chemical mechanical polishing(CMP). The upper surfaces of the through holes filled with conductor 18 become flush with the upper surface of the surrounding insulation layer 15b. Similarly, CMP is carried out also for the lower surface of the Si substrate, to expose the insulation layer 15c and the through holes filled with conductor 18. As a result, a support substrate S having through holes filled with conductor 18 can be obtained.

Please replace the paragraph beginning on page 10, line 13, with the following paragraph.

As a result, the lower electrode and the upper electrode sandwiching a BST dielectric layer form a capacitor. Furthermore, in the region free from the dielectric layer, the lower electrodes and the upper electrodes form through holes filled with conductor. It is preferred that the capacitor electrodes in contact with the oxide dielectric film are made of oxidation resistant material such as Au or Pt, or such material as Pt, Ir, Ru, Pd which keep conductivity even if oxidized, or their oxides.

Please replace the paragraph beginning on page 11, line 12, with the following paragraph.

As shown in 1M, the pattern of the first wiring layer has a pitch and line width corresponding to, for example, one halves of the pitch and line width of the through holes filled with conductor 18. For example, if the through holes filled with conductor have a pitch of 50 mm and a line width of 20 mm, the pattern of the first wiring layer has a pitch of 25 mm and a

line width of 10 mm.

Please replace the paragraph beginning on page 13, line 8, with the following paragraph.

Fig. 2B schematically shows a portion of wires in a module. On the circuit board 50, the intermediate laminate 51 is disposed, and on the intermediate laminate 51, circuit parts 54 including plural semiconductor elements IC1 and IC2 are disposed. In the intermediate laminate 51, there are formed through holes filled with conductor PC formed in the support substrate S, vertical wires WV connected to the through holes filled with conductor PC, electrodes C1 and C2 of a capacitor connected to the vertical wires WV, and local wires LI1 and LI2 for connecting the semiconductor elements with each other.